Simple Architecture for Subsampling LC-based Sigma Delta Modulators

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<td>Ashry, Ahmed; University Pierre &amp; Marie Curie, LIP6 Laboratory Aboushady, Hassan; University Pierre &amp; Marie Curie, LIP6 Laboratory</td>
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Simple Architecture for Subsampling LC-based $\Sigma\Delta$ Modulators

Ahmed Ashry and Hassan Aboushady

In this paper, a simple architecture for subsampling LC-based continuous-time $\Sigma\Delta$ modulators is introduced. The concept of utilizing loop delay to simplify the modulator architecture is generalized to subsampling modulators. Moreover, it is shown that it is possible to remove delay-compensation branch usually used in traditional designs. Removing delay-compensation branch results in a significant simplification of the modulator architecture, and eliminates several problems usually associated with delay-compensation branch.

Introduction: RF Continuous-Time (CT) $\Sigma\Delta$ modulators is a promising solution for realizing RF Analog-to-Digital Converters (ADCs) that are capable of direct digitization of RF signals, and moving most of signal processing to the flexible and programmable digital domain [1]. LC filters are the best candidates for such RF modulators, due to their higher speed and dynamic range, compared to Gm-C and RC filters [2]. However, for LC-based modulators, the number of available nodes for feed-forward or feedback coefficients is half the modulator order, which is not sufficient to implement the desired Noise Transfer Function (NTF) [3].

Additional degrees of freedom can be added by using multi-feedback DAC architectures as in [2, 4]. However, this approach suffers from the increased complexity of the DAC circuitry which is usually accompanied by increased power consumption and thermal noise power.
A simple architecture for LC-based modulators was proposed in [5], where the loop delay was utilized to reduce the number of feedback DAC branches to only three, as shown in Fig. 1. The first branch is the main DAC, which is connected to the input node. The second branch is the internal DAC, which is connected to the internal node. The third branch is the delay-compensation DAC, which is connected directly before the comparator.

In this work, the concept of utilizing loop delay to simplify LC-based modulator architecture is generalized to subsampling modulators. The proposed architecture is even much simpler than original one presented in [5], as it uses only 2 feedback branches instead of two. The proposed architecture also eliminates the need for the delay-compensation branch which is difficult to implement in high speed modulators.

**Subsampling Modulator:** In bandpass CT \( \Sigma \Delta \) modulators, the sampling frequency \( f_s \) is usually 4 times the center frequency of the input signal \( f_o \) to simplify the design of the preceding down-conversion mixer [2]. However, in RF modulators where the center frequency is very high, the required sampling frequency becomes very high and not suitable for available CMOS processes. Subsampling can be used to reduce the sampling frequency to relax the comparator requirements and reduce the power consumption [1, 6].

The architecture proposed in [5] which was shown in Fig. 1 can be extended to subsampling modulator. To find the range of loop delay for which the modulator is stable, the DAC coefficients are calculated for each value of loop delay. Then, the modulator is simulated and the maximum achievable SNR is measured [5]. The DAC coefficients versus loop delay and the corresponding SNR are shown in Fig. 2.
and Fig. 3, respectively.

It can be deduced from Fig. 3 that the subsampling modulator can achieve an acceptable SNR over two ranges of loop delay. The first range of normalized loop delay is from 0 to 0.2, which is too small for practical implementation. The second range is from 0.6 to 0.85, which is suitable for implementation. This means that subsampling modulator is possible to design using the approach proposed in [5] with 3 feedback coefficients.

However, the subsampling has an additional interesting property. As can be seen in Fig. 2, the value of delay-compensation DAC reaches zero when the normalized loop delay is approximately 0.65. This suggests that if the loop delay is kept close to this value, the compensation DAC branch can be removed.

To validate this conclusion, the subsampling modulator was re-designed without the compensation DAC branch as shown in Fig. 4. Then, the DAC coefficients were calculated for each value of loop delay, and the modulator SNR was extracted from simulation, as shown in Fig. 5. It can be concluded from the figure that an acceptable SNR can be obtained over a reasonable range of loop delay. The range of usable loop delay is less wide compared to the first case, because the degrees of freedom is reduced in this case. However, the required range of the loop delay is still feasible to obtain with normal process variations.

Conclusion: The simplified modulator architecture for LC-based CT $\Sigma\Delta$ modulators that was presented before, was generalized to subsampling modulators. The subsampling modulator showed an additional interesting property that made it possible to remove the delay-compensation branch and limit the feedback branches to
only two branches. This simplifies the modulator circuit and eliminates the problems associated with summing node needed for delay-compensation DAC.
References


Figure captions:

Fig. 1 Architecture proposed in [5].

Fig. 2 DAC coefficients versus loop delay in subsampling modulator.

Fig. 3 SNR versus loop delay in subsampling modulator.

Fig. 4 Proposed architecture for subsampling modulator.

Fig. 5 SNR versus loop delay in subsampling modulator without compensation branch.
Authors’ Affiliations:

Ahmed Ashry and Hassan Aboushady, LIP6 Laboratory, University Pierre & Marie Curie, 4 Place Jussieu, 75252 Paris, France.
Email: ahmed.ashry@lip6.fr.
Fig. 2

![Graph showing the relationship between normalized loop delay and currents](image-url)
Fig. 3

![Graph showing the relationship between Max. SNR (dB) and Normalized loop delay (t_d / T).]
Fig. 4

![Block Diagram of an LC Tank Circuit](image-url)
Fig. 5

![Graph showing Max. SNR (dB) vs Normalized loop delay (t_d / T)]