A Designer Centric Analog Synthesis Flow

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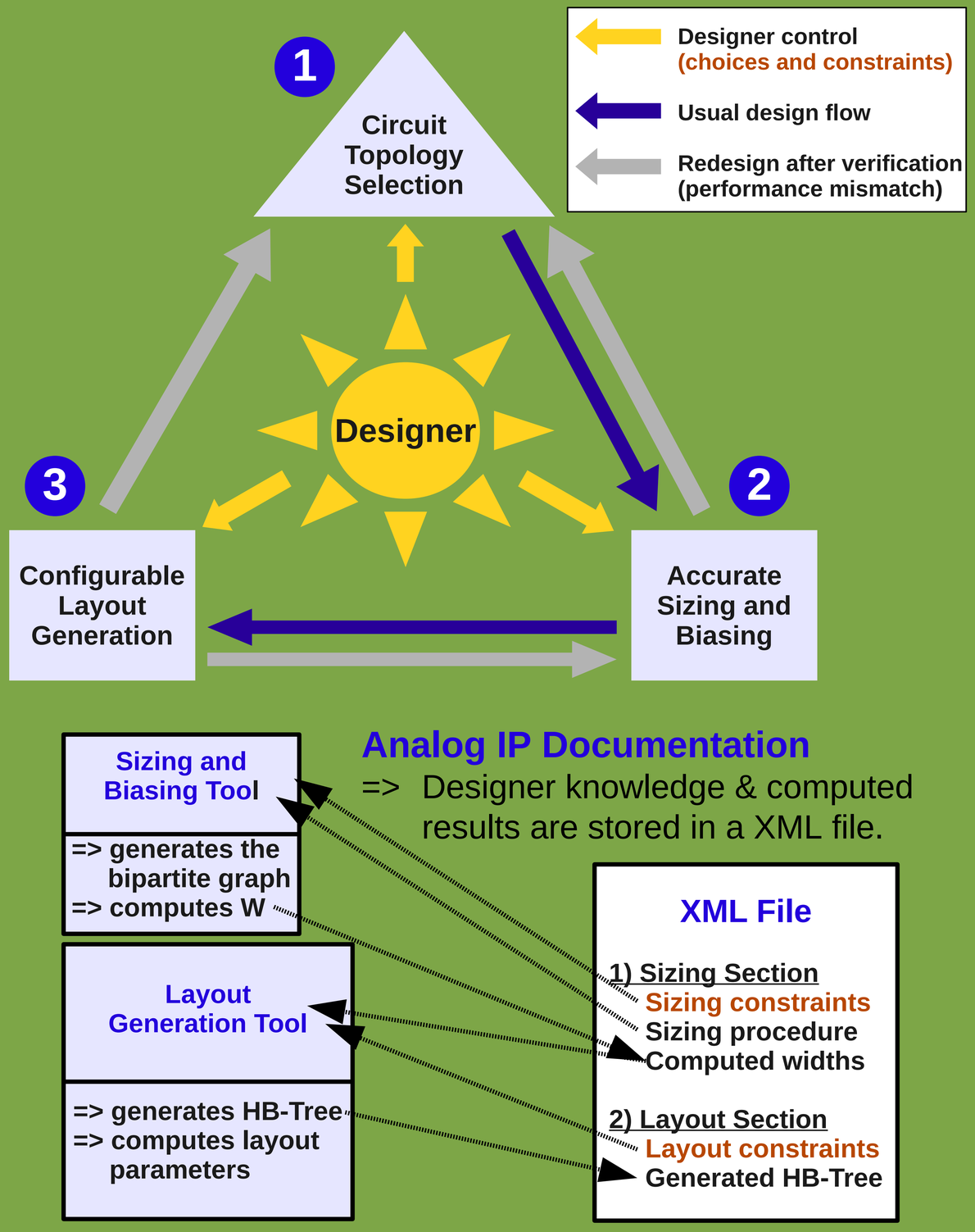
This poster presents a ***designer centric analog synthesis flow*** that is fully controlled by the designer and offers an intuitive design approach. The designer knowledge to conceive an analog IP is the key element of the synthesis flow, it is taken into account to automatically generate the analog IP design procedure and physical view. Thus both consistency and accuracy of the final design are ensured. The presented design flow bridges the gap between the two traditional approaches related to analog design automation, namely the *simulation-based* and the *knowledge-based* approaches, to profit from both approach advantages. The designer centric analog synthesis flow is composed of an **accurate sizing tool** and a **configurable layout generation tool**. Both tools are used to synthesize a fully differential transconductor.



2 Accurate Sizing and Biasing Tool

- Based on the *hierarchical sizing and biasing methodology*
  => sizing procedure generation according to the designer knowledge
- Sizing & biasing operators with standard simulator interface
  => accurate sizing with standard device models (BSIM3v3, BSIM4, PSP, EKV)
- Bipartite graph
  => represents the sizing procedure
  => evaluated from top to bottom to compute transistor sizes

3 Configurable Layout Generation Tool

- Based on Python language
  => concise code to describe complex layout
- Stack object
  => represents the folded transistor
- Routing methodologies
- HB-Tree
  => represents a compact placement

Fully Differential Transconductor Synthesis

The bipartite graphs for each subcircuits (AMP, GMD, CMC) are generated and merged to get the transconductor bipartite graph that is evaluated to compute transistor sizes. These sizes are transmitted to the layout generation tool that takes additional constraints to generate the transconductor layout.