Systematic Design for a Successive Approximation ADC

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Outline

• Background
• Principles of Operation
• System and Circuit Design
• Case Study
  ▫ Simulations
  ▫ Layout Generation
  ▫ Performance Evaluation
• Conclusion
• Perspectives
The Successive Approximation ADC
« The Return »

Emerging new Applications

- MEMS Sensor Interface:
  Resolution: 7-8 bits, BW=50kHz [Scott 2003]
- Multi-standards RF receiver
  Resolution: 8 bits, BW = 20 MHz [Montaudon 2008]
- Ultra Wide Band (wireless UWB):
  Resolution: 5-6 bits, BW=300MHz [Chen 2006]
Figure of Merit

\[
FOM = \frac{P}{2^{\text{Resolution}}} \times 2 \times BW
\]
Objectives

- Develop a systematic design method for successive approximation ADC from system to layout level.
- Develop a general simulation environment with different levels of abstraction and programmed performance analysis.
- Emphasis on analog design automation and reuse techniques:
  - Automatic sizing
  - Layout generation
- Optimizing Layout for best matching
Principle of Operation

$$V_{in} = b_1 \frac{V_{REF}}{2} + b_2 \frac{V_{REF}}{4} + b_3 \frac{V_{REF}}{8} + b_4 \frac{V_{REF}}{16}$$
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Single Ended SAR-ADC.

![Diagram of Single Ended SAR-ADC](image)
Sampling Mode

\[ V_{\text{DAC}} \]

\[ 8C \quad 4C \quad 2C \quad C \quad C \]

\[ V_{\text{REF}} \quad \text{Clock} \quad \text{sample} \quad \text{invert} \]

\[ V_{\text{REF}} \quad V_{\text{DAC}} \quad V_{\text{REF}} \quad V_{\text{In}} \quad V_{\text{In}} \]

\[ V_{\text{in}} \quad V_{\text{REF}} \quad \frac{V_{\text{REF}}}{2} \]

\[ V_{\text{Ref}} \]
Inversion Mode

\[ V_{DAC} = V_{REF} - v_{IN} \]

Clock sample

invert

\[ V_{DAC} \]

\[ V_{REF} \]

\[ v_{IN} \]

\[ V_{REF} - v_{IN} \]
Charge redistribution mode (MSB)
Charge redistribution mode (MSB-1)

\[ V_{\text{DAC}} = V_{\text{REF}} - \text{vin} + \frac{V_{\text{REF}}}{2} + \frac{V_{\text{REF}}}{4} \]

\[ V_{\text{REF}} \]

\[ 8C \quad 4C \quad 2C \quad C \quad C \]

\[ V_{\text{REF}} \]

\[ V_{\text{REF}} \quad \text{sample} \quad \text{invert} \]

\[ V_{\text{REF}} \quad 4 \]

\[ 1 \quad 0 \]
Mode Redistribution de la charge (MSB-2)

\[ V_{DAC} = V_{\text{REF}} - \text{Vin} + \frac{V_{\text{REF}}}{2} + \frac{V_{\text{REF}}}{8} \]

\[ V_{\text{in}} = b_1 \frac{V_{\text{REF}}}{2} + b_2 \frac{V_{\text{REF}}}{4} + b_3 \frac{V_{\text{REF}}}{8} + b_4 \frac{V_{\text{REF}}}{16} \]
Mode Redistribution de la charge (LSB)

\[ V_{\text{DAC}} = V_{\text{REF}} - V_{\text{IN}} + \frac{V_{\text{REF}}}{2} + \frac{V_{\text{REF}}}{8} + \frac{V_{\text{REF}}}{16} \]

\[ V_{\text{DAC}} = V_{\text{REF}} \]

\[ V_{\text{IN}} = b_1 \frac{V_{\text{REF}}}{2} + b_2 \frac{V_{\text{REF}}}{4} + b_3 \frac{V_{\text{REF}}}{8} + b_4 \frac{V_{\text{REF}}}{16} \]

Clock

sample

invert

V_{\text{DAC}}

V_{\text{REF}}
Problem

Selecting $V_{REF} = V_{dd}$ To increase the dynamic range

Leakage when using normal PMOS switch.

Possible Solution: Switched charge-pump [scott03] or Bootstrap [dessouky01]
Possible solutions - Leakage

Since sometimes $V_{DAC}$ value = 1.5 $V_{DD}$
While $V_{G1} = 0$ when $M1$ is ON, $V_{GD,M1}$ exceeds $V_{DD}$
Possible solutions - Reliability

\[ \text{Max OFF} = V_{DD} - V_{tn} \]

\[ 0 < V_{DAC} < 1.5 V_{DD} \]
Possible solutions - Circuitry

Bootstrap [dessouky01]  Modified Shielding Bootstrap
Differential SAR-ADC

\[ V_{\text{in}} \]

Clock

\[ V_{\text{dd}} \]

\[ V_{\text{dd}} \]

Sample

\[ V_{\text{dd}} \]

\[ V_{\text{dd}} \]

Triple Reference
Differential SAR-ADC

\[
\frac{V_{dd}}{2} + \frac{V_{dd}}{2} + \frac{V_{dd}}{4} + \frac{V_{dd}}{8} + \frac{V_{dd}}{16} + \frac{V_{dd}}{2} + \frac{V_{dd}}{2}
\]

\[
\frac{V_{dd}}{2} - \frac{V_{dd}}{2} - \frac{V_{dd}}{4} - \frac{V_{dd}}{8} - \frac{V_{dd}}{16} - \frac{V_{dd}}{2} - \frac{V_{dd}}{2}
\]

Clock

Sample

Invert

DAC2

DAC1

In1

In2

1 0 1 0
Operation - Summary

<table>
<thead>
<tr>
<th>Single Ended Double reference</th>
<th>Differential Triple reference</th>
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<tbody>
<tr>
<td></td>
<td>2 times the numbers of capacitors</td>
</tr>
<tr>
<td></td>
<td>6 times the numbers of switches</td>
</tr>
<tr>
<td>Special Switch (charge-pump - bootstrap)</td>
<td>No need for special switch</td>
</tr>
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<td>Differential architectures advantages:</td>
<td>Differential architectures advantages:</td>
</tr>
<tr>
<td>- Suppressing even harmonics</td>
<td>- Supressing even harmonics</td>
</tr>
<tr>
<td>- Common mode rejection</td>
<td>- Common mode rejection</td>
</tr>
<tr>
<td>- Offset removal</td>
<td>- Offset removal</td>
</tr>
<tr>
<td>Lower power consumption</td>
<td>Better performance at high frequencies</td>
</tr>
</tbody>
</table>
Outline

• Background
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Design - Architecture

- Capacitor array
- Comp
- Control SAR
- Switches Control
- Sample invert

Clock
Capacitor array design issues - Noise

1- Thermal noise \[ \frac{kT}{C_{TOT}} \], due to Sampling

\[ C_{Unit} \text{ increases, thermal noise decreases} \]
Capacitor array design issues - Mismatch

2 – Capacitor Mismatch (Introduced in fabrication)
   - Affects Generated comparison levels of the capacitve DAC

\[ V_{dd} \neq \frac{V_{dd}}{2} \]

\[ V = 8(C + \Delta C) \]

\[ C_{Unit} \text{ increases, mismatch effect decreases} \]
Capacitor array design issues - $f_{\text{Sampling}}$

3- Sampling Frequency

$\tau = R_{\text{Switch}} C_{\text{Total}}$

$t_{\text{sampling}} \approx \frac{T_{\text{Clock}}}{2} \gg \tau$ \quad \text{For an accurate sampling}

$C_{\text{Unit}}$ decreases, bandwidth increases
Switches

1) Switches selection

• NMOS to switch $V_{\text{gnd}}$ and $V_{\text{cm}}$
• PMOS to switch $V_{\text{dd}}$
• CMOS to switch $V_{\text{in}}$
• Bootstrap to force deep off-state of critical switches

2) Sizing switches (compromise)

• Increasing W/L reduces $R_{\text{switch}}$ and so $\tau$, on the account of increasing switch parasitics.
• In the used DAC, this will be of minor importance if operating in low frequency because the switches are all connected to the bottom plates
Design - Architecture

- Capacitor array
- Comp
- Control SAR
- Switches
- Switches Control
- Sample
- invert
- Clock
- In
Comparator Circuit

Reset to Vdd

Cuts the current path in the RESET phase

Input Signal

Latch
Comparator - Operation phases

Reset phase to Vdd

Comparison phase

Inputs

Latch starts

Resolution $> \frac{V_{LSB}}{2}$

Response time $< 0.5 \ T_H$
Comparator - Design tradeoff

Sizing input pair and latch

\( \tau_{latch} \)

Improve with decreasing \( L \)

\( \tau_{init} \)

\( I_{Total} \)

Improve with increasing \( L \)

\( V_{offset} \)

Tradeoff
Design - Architecture

Clock

In

Capacitor array

Switches

Comp

Control SAR

Sample

invert

Switches Control
SAR algorithm - Implementation

LFSR: Linear Feedback Shift Register

<table>
<thead>
<tr>
<th></th>
<th>DAC outputs</th>
<th>C</th>
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<tr>
<td>0</td>
<td>0 0 0 0 0 0 0 0</td>
<td>X</td>
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<tr>
<td>1</td>
<td>1 0 0 0 0 0 0 0</td>
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<td>2</td>
<td>a8 1 0 0 0 0 0 0</td>
<td>a7</td>
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<td>3</td>
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<td>a1</td>
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</table>
Systematic design for SA-ADC

Resolution – BW – Power - Techno

Non idealities and noise
Thermal noise, mismatch, ...

Clock frequency

Switches
Sizing

Cmax

Comparator specs
Settling, resolution, kickback....

Select number of stages

Sizing procedure

Check Specs

Yes

No

Yes

No

Yes

No

Cmax > Cmin

C unity = C min

Layout

System architecture
DAC topology, SAR algorithm, Sampling technique
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Case Study

- Case Study
  - Differential Architecture
  - Resolution: 8bit
  - BW: 50 KHz
  - \( F_{\text{clock}} \): 1MHz
  - Technology: 0.13u ST, MIM Capacitors

- Verification
  - VHDL AMS used for verification with simulation
  - Different levels of abstraction (Behavioral, gates, transistor, …)
  - Mixed blocs simulation (Analog / Digital)
Multiple abstractions
Verification Environment

Verification Environment presets
DAC topology, SAR algorithm, Sampling technique

Abstraction level
Ideal, mismatched, techno, ...

Component sizes

Type of analysis

Resolution – BW

Sketch output spectrum

Calculate SNDR

Sketch SNDR v.s. fin

Sketch SNDR v.s. Ain

Sketch INL and DNL

Sketch Transient response at each node
Transistor level simulations

Vdd 1.2V
Fin 1.4KHz
Fclk 1MHz
Vin_p-p 1.2V
Transistor level simulations

**Transistor level simulations**

Vdd 1.2V
Fin 1.4KHz
Fclk 1MHz
Vin_{p-p} 1.2V
Transient - Differential - DACs

Vdd 1.2V
Fin 1.4KHz
Fclk 1MHz
Vin_{p-p} 1.2V
Transiant - Differential - Comparator

Full conversion: Differential DACs output – Comparator output

Transistor level simulations

Vdd 1.2V
Fin 1.4KHz
Fclk 1MHz
Vin_{p-p} 1.2V
Transient - SAR control

Control block turning ON and OFF DAC switches [case of 0 input]

Vdd 1.2V

Fin 1.4KHz

Fclk 1MHz

Vin_{p-p} 1.2V

VHDL Description
Transient - Full Scale Ramp

Full Scale Slow ramp excitation

Zoom - in
Static Performance - Transistor Level

Static performance Evaluation in (LSB): DNL and INL [16 sample / bin]

(a) DNL vs Code

(b) INL vs Code
Dynamic Performance - Ideal Models

Vdd 1.2V
Fin 1.4KHz
Fclk 1MHz
Vin_{p-p} 1.2V

4096 point FFT

SNDR = 47.47 dB
Dynamic Performance - Mixed Models

Vdd 1.2V
Fin 1.4KHz
Fclk 1MHz
Vin_{p-p} 1.2V

4096 point FFT

SNDR = 47.47 dB

SNDR = 47.44 dB

SNDR = 46.78 dB

SNDR = 46.69 dB
Dynamic Performance - Transistor Level

Vdd 1.2V
Fin 1.4KHz
Fclk 1MHz

1024 point FFT

SNDR = 46.2 dB
**Dynamic Performance**

- $V_{dd} = 1.2V$
- $F_{in} = 1.4KHz$
- $F_{clk} = 1MHz$

4096 point FFT

**Transistor level simulations**

- SNDR max
  - Ideal = 47.47 dB
  - Transistor Level = 46.2
Dynamic Performance

Vdd 1.2V
Fclk 1MHz
Vin_{p-p} 1.2V

4096 point FFT

Signal to noise and distortion ratio SNDR (dB)

Transistor level simulations

BW = 55 KHz
Mismatch analysis

Vdd 1.2V
Fin 1.4KHz
Fclk 1MHz
Vin_p-p 1.2V

4096 point FFT

\[
\text{SNDR} = 46.36 \text{ dB}
\]

\[
\text{SNDR} = 44.13 \text{ dB}
\]
Layout generation for SA-ADC

Comparator transistor sizes

Design phase
- Number of capacitors and sizes
- Desired layout shape
- Unit capacitance
- Common centroid placement algorithm

Layout template s
- Component connectivity
- Relative place and route

CAIRO Layout generation

Target technology

DRC – LVS

Parasitics Ext.

Verification

Fabrication
Layout - Comparator - Floorplan
Area 22 x 39 µm²
Common centroid placement for 16 capacitor

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Layout - Differential DACs - Generated

Layout 1 - 256 Cu – Placed and Routed – Area 1.26 x 0.26 mm² and Huge routing parasitics
Layout - Differential DACs - Manual

Layout 2 - 256 Cu – Placed and Routed – 2/3 less routing parasitics

Area 0.1056 mm²
### Performance

<table>
<thead>
<tr>
<th></th>
<th>[Hong07]</th>
<th>This work*</th>
<th>[scotto03]</th>
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<tbody>
<tr>
<td>Technology</td>
<td>0.18 µm</td>
<td>0.13 µm</td>
<td>0.25 µm</td>
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<tr>
<td>Supply</td>
<td>0.83 V</td>
<td>1.2 V</td>
<td>1.0 V</td>
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<tr>
<td>Input range</td>
<td>Rail to Rail</td>
<td>Rail to Rail</td>
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<tr>
<td>Sampling rate</td>
<td>111 KHz</td>
<td>111 KHz</td>
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<td>Unit Cap.</td>
<td>24 fF</td>
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<td>Power (Analog)</td>
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<td>0.72µW</td>
<td>2.2 µW</td>
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<td>Area</td>
<td>0.062 mm²</td>
<td>0.122 mm²</td>
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<tr>
<td>SNDR@BW</td>
<td>47.40 dB</td>
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Summary and Conclusion

- Systematic design methodology for SA-ADC from system to layout.
- General simulation environment
  - Different abstraction levels.
  - Different verification tests.
- Emphasis on analog design automation and reuse
- Optimizing Layout for best component matching
- Verification with case study for WSN specs
Perspectives

- Targeting high frequency specs (>500 Msample/S)
  - Redundant system error correction code [Kuttner02]
  - Digital calibration [Promitzer01]
  - Asynchronous operation [Chen06]
  - Time interleaving [Chen06]

- Full Automation
  - Sizing procedure with layout parasitics awareness
  - Layout generation for the full ADC
Thank You